Remarks

The Final Office Action has ignored multiple claim limitations by failing to provide or even assert correspondence to limitations in both independent and dependent claims. For these claims to which no correspondence has been asserted, the corresponding rejections are improper, and Applicant believes the claims to be in condition for allowance. Regarding claims to which the Office Action has attempted to assert correspondence, Applicant submits that the Office Action's interpretation of the cited reference is improper, and therefore believes that the reference does not correspond to the claimed invention. Applicant thus believes that all claims are allowable over the cited reference. The following more particularly addresses these matters.

The Final Office Action dated August 13, 2008, indicated that: figures 2-4 stand objected to; and claims 1-29 stand rejected under 35 U.S.C. § 102(b) over Schwarz (U.S. Patent No. 6,496,947). Applicant traverses all rejections, and further does not acquiesce to any rejection or averment in this Office Action unless expressly indicated otherwise.

Applicant respectfully traverses all Section 102 rejections because the cited memory cell and BIST controller of the '947 reference do not respectively correspond to the claimed functional device and integral characterization unit (as in independent claims 1, 20 or 23). In general, the Office Action has misconstrued the disclosure in the '947 reference, in which the cited BIST 18 directly generates test stimuli for a memory array 12, and thus does not provide correspondence to limitations directed to an integral characterization unit that controls a functional device where the functional device operates in response to other test stimuli. In short, the Office Action has confused and/or combined "test stimuli" with control signals that control a circuit to respond to the test stimuli. In this context, the rejections are also unclear as to what is being asserted as corresponding to the claimed functional device and its operation in response to test stimuli, and to the claimed control of the functional device by an integral characterization unit. Referring to FIG. 1 and column 3:61-4:27 of the '947 reference, the BIST circuit 18 actually provides test inputs (memory read) to the memory cell 12 during a test mode, and the memory cell 12 does not receive any separate test stimuli. The rejections have therefore failed to show correspondence to these limitations.

Further regarding independent claim 20, the Office Action has alleged no correspondence to the claimed "built-in test hardware providing functional test data" or the "controller that controls the integral characterization unit and the built-in test hardware," on the same semiconductor device with the described BIST circuit 18 or otherwise. Moreover, the Office Action has not shown that the cited BIST circuit 18 includes variable voltage and clock controllers and provides "characterization test data." The Office Action's citation to the "memory tester 250" at page 4 of the Office Action is erroneous because this tester is not part of the BIST circuit 18, which is alleged as corresponding to the integral characterization unit. This memory tester 250 is a "factory test apparatus" that is used externally from the integrated circuit 10 that is being tested, and is coupled to various inputs and outputs as shown in FIG. 1. This memory tester 250 does not correspond, for example, to the claimed invention as exemplified in embodiments including those shown in FIG. 3 of the instant application, where voltage and clock controllers 307 and 309 are part of the chip 301 but separate from BIST 305. These controllers in FIG. 3 separately provide voltage/clock signals to the device under characterization (DUC) and the BIST 305. The Office Action has thus also failed to show correspondence to related voltage or clocking-type limitations in dependent claims 3, 4, 8, 28 and 29, and to related built in test hardware-type limitations as in dependent claims 13-17.

In view of the above, the Office Action has failed to show correspondence to limitations in each of the independent claims and, correspondingly, to the claims that depend therefrom.

As discussed above, no correspondence has been shown to limitations directed to voltage and/or clock control in claims 3, 4, 8, 25-26, 28 and 29, or to the built in test hardware-type limitations in claims 13-17. The Office Action has also failed to assert any correspondence whatsoever to multiple other dependent claim limitations, with certain of these limitations discussed here by way of example.

Regarding claim 5, the Office Action has not asserted any disclosure of the claimed integral characterization unit as controlling a functional device that separately receives test stimuli, or that receives test stimuli from an external source. As discussed above, '947 reference uses its BIST controller to generate test inputs (reads and writes)

that are supplied to the memory array 12, whereas any external inputs to the memory array are not carried out during a test function (*i.e.*, the BIST circuit 18 is disabled during normal operation as discussed at column 3:48-52). In this regard, the Office Action has not asserted, and the '947 reference does not disclose, limitations directed to a functional device that "receives the test stimuli directly from an external source."

Regarding claims 18 and 21, the Office Action has cited no reference that provides correspondence to limitations directed to a memory module to store characterization data of a functional device.

Regarding claim 27, the office Action has not cited any correspondence to limitations directed to an integral characterization unit that controls a functional device to provide characterization data including "minimum and maximum operating voltage, minimum and maximum operating temperature, and minimum and maximum operating clock frequencies." Applicant has further reviewed the '947 reference and cannot ascertain any disclosure of these limitations. Moreover, it appears that the cited BIST cannot operate to provide such characterization of the memory array 12.

In view of the above, Applicant submits that all claim rejections are improper and requests that they be removed.

Applicant believes that the objections to the drawings are no longer applicable in view of the replacement sheets filed herewith.

In view of the above, Applicant believes that each of the objections and rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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Attachment: Two Replacement Drawing Sheets